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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,192	EVANS ET AL.	
	Examiner	Art Unit	
	Kathleen S. Yuan	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The response received on 4/23/2007 has been placed in the file and was considered by the examiner. An action on the merit follows.

Response to Amendment

1. The amendments filed on 23 April 2007 have been fully considered. Response to these amendments is provided below.

Summary of Arguments/Amendments and Examiner's Response:

2. The applicant has amended the claims to emphasize the moving of the wafer along the path in conjunction with the camera, along with amending the some of the claims to include a limitation that the image is interlaced. Additionally, the applicant has added new claims to the application

3. The applicant has argued that Rostami is an improper combination with a surface inspection apparatus or measurement system, since surface inspection apparatuses and measurement systems do not need to identify an orientation in the wafer.

4. The examiner disagrees with this statement. Surface inspection apparatuses need to identify the orientation of a wafer because it needs to find that the wafer is being imaged in the way the system desired. By finding the orientation of the wafer, the system can properly image a wafer. Furthermore, a measurement system needs the orientation as well. It would be difficult if not impossible to make a measurement of the image properties of a subject without ensuring that the subject is properly oriented for

imaging. Therefore, by finding the orientation of the wafer, the system is more robust, since the most accurate image is found for processing.

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 28 recites the limitation "the sequentially taken line images" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 29 recites the limitation of "the wafer image" that is separated in line 2. It is unclear as to which wafer image the applicant is referring to, since claim 1 states that the wafer images are the separated images already. The examiner thinks that the applicant intends to state that the line images are the "the wafer image" of claim 29, since that is what is separated in claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 8-11, 13-14 and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6937753 (O'Dell et al) in view of U.S. Patent No. 5064291 (Reiser).

Regarding claim 1, O'Dell et al discloses an apparatus comprising: a camera positioned along the path of travel, since the wafer is moving, (col. 8, line10-11) for taking a plurality of line images of different portions of the wafer across a substantial portion of the wafer in succession (col. 8, lines 12-20) as the wafer moves along the path of travel (col. 8, lines 14-15); an illumination device positioned along the path of travel (col. 8, line 30-31) for projecting at least two different types of illumination, brightfield and darkfield illumination (col. 11, lines 52-55) and no illumination at all since the lights blink (col. 8, lines 30-31), along the path of travel intersected by the wafer in the area that the line images are taken (col. 8, lines 29-33), the illumination device is adapted to change the type of illumination in a synchronous manner, a blinking manner as a strobe light (col. 8, lines 30-31) with the taking of the plurality of line images; and a processor (fig. 8, item 26) in electronic communication with the camera (fig. 8, item 20) for identifying the wafer marking, or a defect, on at least one of the wafer images of different illumination by inspecting the wafer and identifying where the defect is (fig. 2, item c), and reading the wafer mark, by reviewing the defect and reading the defect again (fig. 2, item D).

O'Dell et al does not disclose expressly that the processor in electronic communication with the camera is for separating the line images into at least two separate wafer images of different illumination.

Reiser discloses that a processor (fig. 11, item 78) in electronic communication with the camera (fig. 11, item 72) is used for separating the line images into at least two separate wafer images of different illumination (col. 3, lines 42-43)

O'Dell et al and Reiser are combinable because they are from the same field of endeavor, i.e. inspection with variable illumination.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to separate the line images into the two different types of illumination.

The suggestion/motivation for doing so would have been to provide a more accurate system by highlighting different characteristics with the different illumination types clearly.

Therefore, it would have been obvious to combine the apparatus of O'Dell et al with the changing of illumination and separating of images of Reiser to obtain the invention as specified in claim 1.

12. Regarding claim 8, Reiser discloses that the processor includes a first computer software component that receives the line images from the camera (fig. 11, item 82).

13. Regarding claim 9, Reiser discloses that a processor contains the software, since programs are stored there (fig. 11). Therefore, any action carried out has a software component/ program. Reiser further discloses that all the units are in electronic communication, as seen in fig. 11. O'Dell discloses this as well when disclosing that all

the actions of lights, imaging and path are connected (col. 8, lines 10-35). The illumination device is monitored to correlate with the speed of the plate (col. 8, line 30-31), the movement of the path of travel is monitored (col. 8, lines 14-15), and the rate of the path of travel is monitored as well (col. 8, line 31) to correlate with the illumination.

14. Regarding claim 10, Reiser discloses that software components control the different actions of the system (fig. 11, item 88), and O'Dell discloses that actions of the system include the use of the illumination device, movement of the line path of travel and the rate of the path of travel respectively (col. 8, lines 11-34).

15. Regarding claim 11, Reiser discloses that a processor contains the software, since programs are stored there (fig. 11). Therefore, any action carried out has a software component/ program. O'Dell et al discloses locating an identifiable area wherein the wafer markings are located (col. fig. 2, item C and fig. 5, item C7).

16. Regarding claim 13, O'Dell et al discloses a sixth software component for reading the wafer mark (fig. 2, item D and fig. 6).

17. Regarding claim 14, O'Dell et al discloses an apparatus comprising: a camera positioned along the path of travel, since the wafer is moving, (col. 8, line10-11), the camera adapted to take a plurality of individual and sequential line images of different portions of the wafer in succession across substantially the entire silicon wafer surface as the wafer moves along on the path of travel (col. 8, lines 12-20); an illumination device positioned along the path of travel (col. 8, line 30-31) for projecting at least two different types of illumination, brightfield and darkfield illumination (col. 11, lines 52-55) and no illumination at all since the lights blink (col. 8, lines 30-31), along the path of

travel intersected by the wafer in the area that the line images are taken (col. 8, lines 29-33), the illumination device is adapted to change the type of illumination in a synchronous manner, a blinking manner as a strobe light (col. 8, lines 30-31) with the taking of the plurality of the sequential line images; and a processor (fig. 8, item 26) in electronic communication with the camera (fig. 8, item 20) and illumination devices (col. 8, lines 29-30) for locating the wafer marking, or a defect, on at least one of the wafer images of different illumination by inspecting the wafer and identifying where the defect is (fig. 2, item c), and reading the wafer mark, by reviewing the defect and reading the defect again (fig. 2, item D).

O'Dell does not expressly disclose that a single interlaced image of the wafer is found and that the processor in electronic communication with the camera and the illumination device is adapted to separate the single interlaced wafer image into separate images having the same type of illumination.

Reiser discloses that a single interlaced image of the wafer is found in an array (fig. 11, item 90 and col. 2, line 66- col. 3, line 1) and that the processor in electronic communication with the camera and the illumination device (fig. 11, items 78, 72 and 74, respectively) is adapted to separate the single interlaced wafer image into separate images, the images having the same type of illumination within the image (col. 3, lines 42-44).

18. Regarding claim 28, Reiser discloses that the processor is adapted to generate a single interlaced image of the object under inspection, an array (col. 2, lines 66-68).

O'Dell discloses that the images are taken under alternating illumination (col. 8, lines 30-31).

19. Regarding claim 29, Reiser discloses that the separation of the line images having the same illumination type occurs as the sequential line images are taken since the colors of illumination are part of the separation and this occurs when images are taken (col. 3, lines 28-46) and produces at least two wafer images each image having the same illumination type (col. 3, lines 46-47).

20. Regarding claim 30, O'Dell et al discloses an apparatus comprising: an illumination device (col. 8, line 30-31) positioned along the path of travel adapted to alternatingly project at least two different types of illumination, brightfield and darkfield illumination (col. 11, lines 52-55) and no illumination at all since the lights blink (col. 8, lines 30-31), across the wafer in succession as the wafer moves along the path of travel (col. 8, line 31-32), an image recording device positioned along the path of travel adapted to take a plurality of sequential line images of the wafer (col. 8, line 11-20) synchronous with the alternating types of illumination (col. 8, line 29-33); and a processor (fig. 8, item 26) in electronic communication with the image recording device (fig. 8, item 20) adapted to identify and read the wafer markings, or a defect, on at least one of the wafer images of different illumination by inspecting the wafer and identifying where the defect is (fig. 2, item c), and reading the wafer mark, by reviewing the defect and reading the defect again (fig. 2, item D)..

O'Dell et al does not expressly disclose that the processor that is in electronic communication to the image recording device is adapted to separate the sequential line images having the same type of illumination.

Reiser discloses that the processor that is in electronic communication to the image recording device (fig. 11, items 78, 72, respectively) is adapted to separate the single interlaced wafer image into separate images, the images of a type of illumination separated from the images of another type (col. 3, lines 42-44).

21. Claims 31 and 32 are rejected for the same reasons as claims 28 and 29. Thus, the arguments analogous to that presented above for claims 28 and 29 are equally applicable to claims 31 and 32. Claims 31 and 32 distinguishes from claims 28 and 29 only in that they have different dependencies, both of which have been previously rejected. Therefore, prior art applies.

22. Claims 15, 17 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser, as applied to claims 1, 14 and 30 above, and further in view of U.S. Patent No. 5861910 (McGarry et al).

Regarding claim 15, O'Dell discloses a method comprising: generating images of a wafer image through separately and sequentially taking a plurality of line images of different portions of the wafer in rapid succession across substantially the entire surface of the wafer (col. 8, lines 11-20, as explained above for claims 1, 14 and 30) and synchronously and sequentially projecting alternating types of illumination in the area of the line image (col. 8, lines 30-31) producing the images of the sequential line images of

alternating types of illumination (col. 8, lines 29-34); locating an area on the wafer containing the wafer markings, in the case of O'Dell, the wafer markings being a defect; (fig. 2, item c and all steps before item C because they lead to the locating), and reading the wafer mark, by reviewing the defect and reading the defect again (fig. 2, item D).

O'Dell et al does not expressly disclose that the images are a single interlaced image and that the wafer markings can be markings to identify the wafer.

Reiser discloses that a single interlaced image of the wafer is found in an array (fig. 11, item 90 and col. 2, line 66- col. 3, line 1), which is interlaced because both illumination types are interlaced with each other in the image (col. 3, lines 42-44).

O'Dell et al and Reiser are combinable because they are from the same field of endeavor, i.e. inspection with variable illumination.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have a single interlaced image.

The suggestion/motivation for doing so would have been to provide a faster scanning system by only scanning one image instead of stopping in between and scanning separate images.

O'Dell et al (as modified by Reiser) does not disclose expressly that markings identify a wafer.

McGarry et al discloses that a wafer mark can be an indicia that identifies a wafer (col. 1, lines 34-36).

O'Dell et al (as modified by Reiser) and McGarry et al are combinable because they are from the same field of endeavor, i.e. wafer inspection.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to locate a wafer marking that identified the wafer.

The suggestion/motivation for doing so would have been to provide a more robust method of allowing a system to automatically find the identity of the wafer.

Therefore, it would have been obvious to combine the method of O'Dell et al (as modified by Reiser) with the wafer marking indicia of Reiser to obtain the invention as specified in claim 15.

23. Regarding claim 17, O'Dell et al discloses a method comprising, generating at least one wafer image comprising a plurality of separately and sequentially taken line images of different portions of the wafer across a substantial portion of the wafer as the wafer moves along the path of travel wafer (col. 8, lines 11-20, as explained above for claims 1, 14 and 30), locating an area containing the wafer markings on the at least one wafer image, in the case of O'Dell, the wafer markings being a defect; (fig. 2, item c), and reading the wafer markings, by reviewing the defect and reading the defect again (fig. 2, item D).

O'Dell et al does not expressly disclose that the line images are interlaced and that reading wafer markings identify the wafer.

Reiser discloses that a single interlaced image of the wafer is found in an array (fig. 11, item 90 and col. 2, line 66- col. 3, line 1), which is interlaced because both illumination types are interlaced with each other in the image (col. 3, lines 42-44).

O'Dell et al (as modified by Reiser) does not disclose expressly reading wafer markings to identify the wafer.

McGarry et al discloses that a wafer mark can be an indicia that identifies a wafer (col. 1, lines 34-36).

24. Regarding claim 24, O'Dell et al discloses the step of providing alternatingly (col. 8, lines 30-31), since the lighting alternatingly strobes, and synchronously (col. 8, lines 30-31), since the lighting is synchronous to the speed (col. 8, lines 30-34) of different types of illumination on the wafer for each line image taken (col. 8, lines 10-20).

25. Regarding claim 25, Reiser discloses the step of separating the sequentially taken line images into at least two wafer images each wafer image having the same type of illumination (col. 3, lines 42-44).

26. Regarding claim 26, Reiser discloses that the separation of the line images having the same illumination type occurs as the sequential line images are taken since the colors of illumination are part of the separation and this occurs when images are taken (col. 3, lines 28-46) and produces at least two wafer images each image having the same illumination type (col. 3, lines 46-47).

27. Regarding claim 27, Reiser discloses that the at least one wafer image comprises a single interlaced image of the line images having different illumination because the image has different illuminations interlaced within each other (col. 3, lines 42-44). O'Dell discloses that the line images are sequential (col. 8, lines 10-20).

28. Claims 1, 14, and 30 can also be rejected under the three references if interpreting that the wafer marking must be an indicia that identifies a wafer by rejecting the claims in the same fashion disclosed for the claim rejections of claims 1, 14 and 30

above, and adding the reference of McGarry that discloses a wafer mark can be an indicia that identifies a wafer.

29. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser, as applied to claim 1 above, and further in view of U.S. Patent No. 5455870 (Sepai et al).

Regarding claim 4, O'Dell et al (as modified by Reiser) discloses all of the claimed elements as set forth above and incorporated herein by reference. O'Dell et al further discloses that the camera is adapted to respectively take both sequential (col. 8, lines 11-20) and synchronous images (col. 8, lines 29-34) with the changing type of illumination (col. 8, lines 30-31).

O'Dell et al (as modified by Reiser) does not disclose expressly that the camera further comprises at least two individual cameras positioned adjacent one another and transverse the path of travel.

Sepai et al discloses that a camera that obtains different types of illumination (bright field and dark field, fig. 2, items 32 and 22) is comprised of two individual cameras positioned adjacent one another (fig. 1, items 24 and 34) that transverse the path of travel, since the stage can move in the x and y direction in respect to the cameras.

O'Dell et al (as modified by Reiser) and Sepai et al are combinable because they are from the same field of endeavor, i.e. inspection using different types of illumination.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have two separate cameras for the one camera.

The suggestion/motivation for doing so would have been to provide a simplified faster system by allowing the separation to occur when taking the images, by skipping the processing of separating the two colors in Reiser.

Therefore, it would have been obvious to combine the apparatus of O'Dell et al (as modified by Reiser) with the two cameras of Sepai et al to obtain the invention as specified in claim 4.

30. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser, as applied to claim 1 above, and further in view of U.S. Patent No. 6075883 (Stern et al).

Regarding claim 5, O'Dell et al (as modified by Reiser) discloses all of the claimed elements as set forth above and incorporated herein by reference. Reiser further discloses that the at least two different types of illumination include a bright field illumination, a dark field illumination (fig. 7, items 50 and 52),

O'Dell et al (as modified by Reiser) does not disclose expressly that the illumination includes an incandescent illumination and LED illumination.

Stern et al discloses that brightfield and darkfield illumination (col. 4, lines 25-31) can use LEDs (col. 5, line 4) and incandescent illumination (col. 5, line 3).

O'Dell et al (as modified by Reiser) and Stern et al are combinable because they are from the same field of endeavor, i.e. lighting in inspection systems.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use LEDs and incandescent illumination.

The suggestion/motivation for doing so would have been to provide a more robust, user-friendly system by providing a well-known way of illumination, thus allowing an easy fix in case the lighting is corrupted by simple replacement.

Therefore, it would have been obvious to combine the apparatus of O'Dell et al (as modified by Reiser) with the lighting of Stern et al to obtain the invention as specified in claim 5.

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser, as applied to claim 1 above, and further in view of U.S. Patent No. 5825913 (Rostami et al).

Regarding claim 12, O'Dell et al (as modified by Reiser) discloses all of the claimed elements as set forth above and incorporated herein by reference. Reiser further discloses that a processor contains the software, since programs are stored there (fig. 11), which carry out the processes of the system. O'Dell et al further discloses the need to align a wafer (fig. 5, item C5), and that a center of the wafer is located (col. 9, lines 53-54) and something like an edge notch is found as well (col. 9, line 59). O'Dell et al further discloses that an area containing the wafer markings is located (fig. 6, item c7).

O'Dell et al (as modified by Reiser) does not disclose expressly locating an edge of the wafer and an edge notch of the wafer, calling it an edge notch.

Rostami discloses locating an edge of the wafer (col. 4, lines 15-18) and an edge notch of the wafer (col. 6, line 23 and fig. 2), and further discloses also finding the center of the wafer (col. 3, lines 44-45) and an area containing wafer markings (col. 2, line 35-36).

O'Dell et al (as modified by Reiser) and Rostami are combinable because they are from the same field of endeavor, i.e. inspection systems for wafers.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the edge and notch edge for alignment.

The suggestion/motivation for doing so would have been to provide a more robust system by providing the best possible alignment and thus the best possible images for processing.

Therefore, it would have been obvious to combine the apparatus of O'Dell et al (as modified by Reiser) with the alignment marks of Rostami et al to obtain the invention as specified in claim 12.

32. Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser and McGarry et al, as applied to claims 16 and 17 above, and further in view of Rostami et al.

Regarding claim 16, O'Dell et al (as modified by Reiser and McGarry et al) discloses all of the claimed elements as set forth above and incorporated herein by reference. Reiser further discloses that the step of locating an area on the wafer containing the wafer markings further comprises separating the single wafer image into

individual wafer images having the same illumination (col. 3, lines 42-44). O'Dell et al discloses examining all the images to locate a center of the wafer (col. 9, lines 53-54) and something like an edge notch is found as well (col. 9, line 59).

O'Dell et al (as modified by Reiser and McGarry et al) does not disclose expressly locating an edge and a notch on the edge, calling it specifically an edge notch.

Rostami discloses locating an edge of the wafer (col. 4, lines 15-18) and an edge notch of the wafer (col. 6, line 23 and fig. 2), and further discloses also finding the center of the wafer (col. 3, lines 44-45) and an area containing wafer markings (col. 2, line 35-36).

O'Dell et al (as modified by Reiser and McGarry et al) and Rostami are combinable because they are from the same field of endeavor, i.e. inspection systems for wafers.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the edge and notch edge for alignment.

The suggestion/motivation for doing so would have been to provide a more robust system by providing the best possible alignment and thus the best possible images for processing.

Therefore, it would have been obvious to combine the method of O'Dell et al (as modified by Reiser and McGarry et al) with Rostami to obtain the invention as specified in claim 16.

33. Claim 20 is rejected for the same reasons as claim 16. Thus, the arguments analogous to that presented above for claim 16 are equally applicable to claim 20. Claim 20 distinguishes from claim 16 only in that they have different dependencies and claim 20 is a broader version of claim 16. Since all the limitations are addressed above for claim 16, and both independent claims have been equally rejected, prior art applies.

34. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Dell et al in view of Reiser and McGarry et al, and further in view of Stern et al.

Regarding claim 21, O'Dell et al (as modified by Reiser and McGarry et al) discloses all of the claimed elements as set forth above and incorporated herein by reference.

O'Dell et al (as modified by Reiser and McGarry et al) does not disclose expressly the step of conducting a geometric transform of the area containing the wafer markings prior to reading the wafer markings to improve visibility of the markings.

Stern et al discloses a method of obtaining a composite image of a semiconductor for inspection (col. 6, lines 24-27) to provide a best image that improves visibility of markings (col. 2, lines 49-56) by conducting a geometric transform of the area containing the wafer (col. 4, line 52- col. 11, line 11).

O'Dell et al (as modified by Reiser and McGarry et al) and Stern et al are combinable because they are from the same field of endeavor, i.e. image acquisition in inspection systems.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to provide a geometric transform of the object.

The suggestion/motivation for doing so would have been to provide the best recognition/ identification of markings by providing the best representation of the object.

Therefore, it would have been obvious to combine the method of O'Dell et al (as modified by Reiser and McGarry et al with the transforms of Stern et al to obtain the invention as specified in claim 21.

35. Regarding claim 22, Stern et al discloses examining each of the separated images, the brightfield and darkfield image for entropy (col. 10, lines 32-40) and conducting a geometric transform on the area containing the wafer markings on each of the separated wafer images having different illumination by dividing the area into subpictures (col. 10, lines 34-35), inverting the subpicture (col. 11, lines 2-10), and even conducting the entropy calculation (col. 10, lines 41-49) to provide a best image for inspection (col. 6, lines 24-27). O'Dell et al discloses individually examining the areas containing the wafer markings to determine if the wafer markings can be read on any one of the areas containing the wafer markings by locating the wafer markings and thus determining the wafer markings can be read when they are located (fig. 2, item c).

36. Regarding claim 23, Stern et al discloses combining at least two of the separated, differently illuminated and transformed areas containing the wafer markings (col. 10, lines 25-27) for inspection (col. 6, lines 24-27). O'Dell discloses determining if the wafer markings can be read in the best image, that being the one of Stern, housing the markings (fig. 2, item c).

Conclusion

37. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kathleen S. Yuan whose telephone number is (571)272-2902. The examiner can normally be reached on Monday to Thursdays, 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on (571)272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KY
5/24/2007

JOSEPH MANCUSO
SUPERVISORY PATENT EXAMINER